DC characteristics of InAs/AlSb HEMTs at cryogenic temperatures

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Abstract

The DC properties of 110-nm gate-length InAs/AlSb-based HEMTs at cryogenic (30K) and room temperature (300K) have been investigated. Compared to 300K, devices at 30 K exhibited lower on-resistance (R_{ON}) and output conductance (g_{DS}), a higher transconductance (g_m) and a more distinct knee in the $I_{DS}(V_{DS})$ characteristics. The improvement in the DC performance at cryogenic temperature should mainly be attributed to the lower source-drain resistance.

I. Introduction

InAs/AlSb HEMTs are characterized by higher electron mobility and peak velocity in the active channel layer compared to InGaAs/InAlAs HEMTs [1]. Such characteristics make InAs/AlSb HEMTs potentially interesting in millimetre-wave applications e.g. space communication systems and radio astronomy where low power dissipation and low noise figure are required. Since the signal amplitude in long range space communication is extremely weak, it is necessary to reduce the noise contribution of the receiver by cryogenic cooling of the low-noise amplifier.

The DC and RF performance are sensitive to the operating temperature, especially in 2DEG based devices, due to the contact resistance, electron transport improvements and reduction of thermal noise. Very little has been reported on cryogenic device properties in InAs/AlSb HEMTs [2]. In this paper we have studied the DC performance at cryogenic temperature by measuring InAs/AlSb based HEMTs at 300 K and 30 K.

II. Experiment

The InAs/AlSb HEMT fabrication started with a heterostructure grown by molecular beam epitaxy on a semi-insulating InP substrate. The heterostructure is shown in Fig. 1. Mesa isolation was performed by Cl_2:Ar ICP/RIE dry etching. Pt/Pd/Au ohmic contacts were then deposited and subsequently annealed at 275ºC.

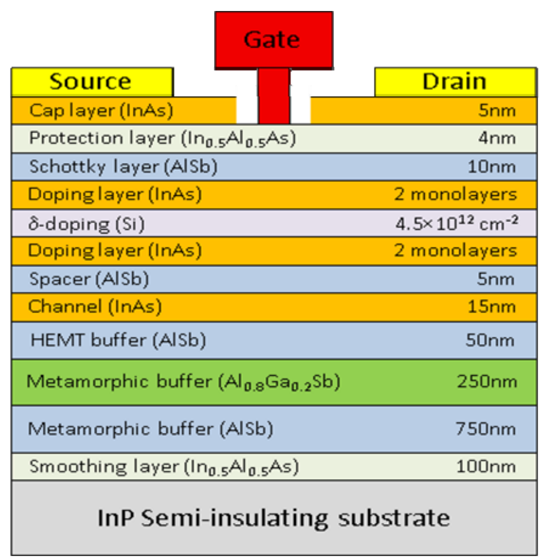

Fig. 1: Epitaxial structure of the 110-nm InAs/AlSb HEMT. The spacer thickness between the barrier and the channel is 5 nm and the effective gate-to-channel distance is 20 nm.

The Ti/Pt/Au T-shaped gates with gate length L_g=110 nm were defined in a two-layer resist by electron beam lithography.

The 5 nm deep gate-recess etch was performed by a citric-acid based wet etchant prior to gate metallization. Finally, a SiN passivation layer was deposited to protect the devices and an ICP/RIE dry etching step was used to expose the metallic pads. DC measurements were then performed.

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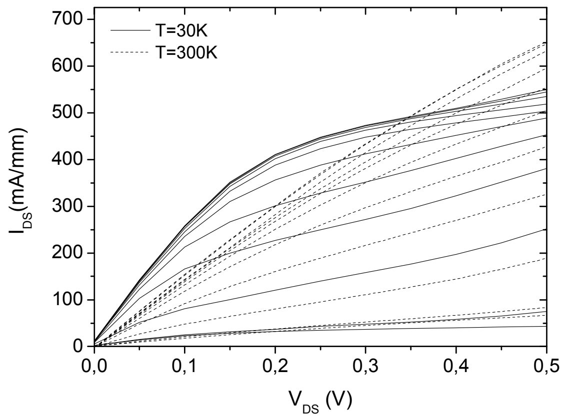

Fig. 2: Drain current (I_{DS}) as a function of drain voltage (V_{DS}) with gate voltage (V_{GS}) ranging from 0.1 V to -1.4 V at 300 K (dashed lines) and 30 K (solid lines).The device gate width is 2x50μm.

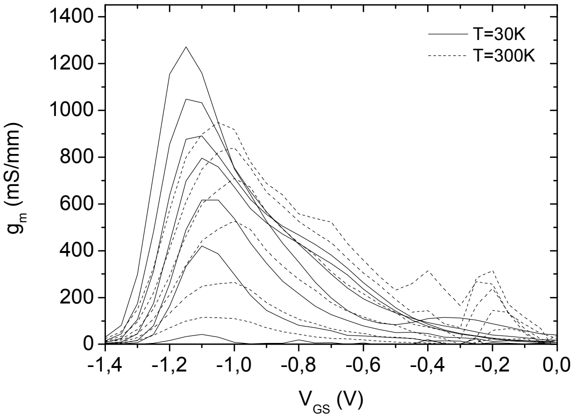

Fig. 3: Transconductance (g_m) as a function of gate voltage (V_{GS}) with drain voltage (V_{DS}) ranging from 0 V to 0.5 V at 300 K (dashed lines) and 30 K (solid lines).

The effective gate-to-channel distance of 20 nm is defined as the total thickness of the Schottky layer, protection layer, the spacer thickness including a doping layer of approximately 1 nm. Transmission line model (TLM) test structures characterization was carried out at room temperature to evaluate the contact resistance R_c and the sheet resistance R_{sh}. The values obtained were 0.07 Ωmm and 108 Ω/□, respectively.

III. Results and discussion

The device reported here is a two finger HEMT with a total gate width of 100 μm. All the measurements at both room temperature (300 K) and cryogenic temperature (30 K) were performed on the same device. The drain current as a function of drain voltage was first measured at 300 K ; See Fig. 2. The on-resistance observed was about 0.5 Ωmm. The f_t and f_{max} was 190 GHz and 170 GHz, respectively. These values represent typical state-of-the-art [3] numbers for an InAs/AlSb HEMT with L_g=110 nm. The DC measurements were carried out at 30 K using a cryogenic probe station. At this temperature, the observed device behaviour was clearly different showing a lower R_{ON} (about 0.3 Ωmm) and higher I_{DS} at low V_{DS}; See Fig. 2. This behaviour is mainly due to the reduction of the source-drain resistance. In particular, the output conductance g_{DS} was reduced at low V_{DS} and high I_{DS}. Furthemore, the device developed a more distinct knee in the I_{DS} versus V_{DS} with no observed kink behaviour.

In Fig. 3 the transconductance at both 300 K and 30 K is shown. The drain voltage V_{DS} was varied from 0 V to 0.5 V. The measurement at 300 K showed a maximum peak g_m of about 950 mS/mm at V_{GS}=-1.1 V and V_{DS}=0.5 V. When the same measurement was repeated at 30 K, an increased peak transconductance g_m of 1280 mS/mm was observed. The g_m curve was also slightly shifted towards higher negative gate bias. Higher g_m indicates a better gate control of the current and a possible increment of the average carrier velocity. This enhancement in peak g_m at 30 K can then be attributed not only to the lower source-drain resistance but possibly also to the lower transit time under the gate because of phonon scattering suppression compared with the 300 K values [4].

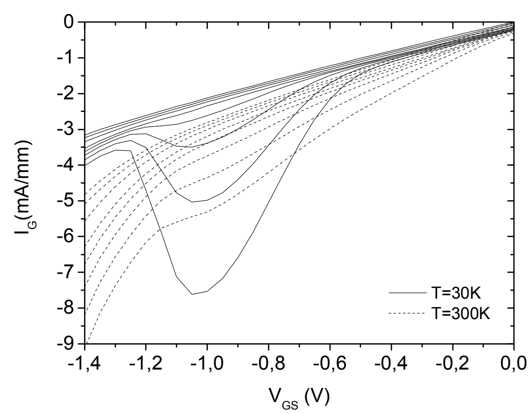

Fig. 4: Gate current (I_G) as a function of gate voltage (V_{GS}) with drain voltage (V_{DS}) ranging from 0 V to 0.5 V at 300 K (dashed lines) and 30 K (solid lines).

The maximum gate leakage current I_{GS} measured at 300 K was 900 μA (9 mA/mm) for V_{GS} =-1.4 V; See Fig. 4. The same measurement performed at 30 K shows a lower gate leakage of 400 μA (4 mA/mm) for V_{GS} = -1.4 V. The overall improvement could be explained by a lower impact ionization effect at high negative gate bias above 1 V. The improved DC properties of InAs/AlSb HEMTs at 30 K compared to 300 K points to the potential of this technology in cryogenic low-

noise amplifier applications operating at low DC power dissipation.

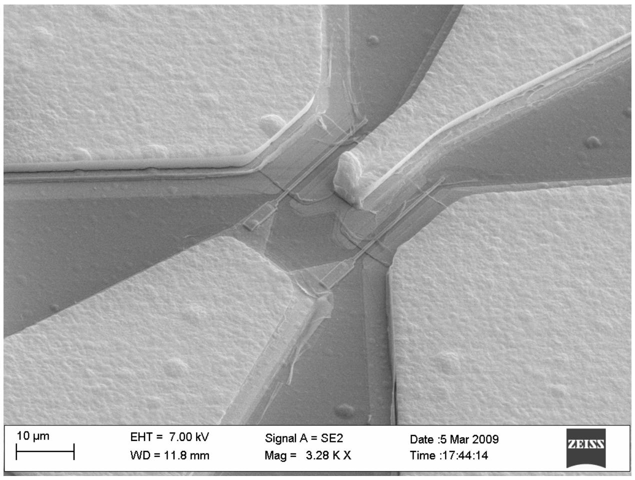

Fig. 5: SEM image showing the 2x50µm InAs/AlSb HEMT.

A scanning electron microscopy (SEM) image of the two finger InAs/AlSb HEMT is shown in figure 5.

III. Conclusions

We have demonstrated that the DC performance for a 110-nm gate-length InAs/AlSb HEMT is clearly improved at cryogenic temperature compared to room temperature. In particular, the on-resistance decreased from about 0.5 Ωmm to about 0.3 Ωmm due to the lower source-drain resistance and the maximum transconductance increased from 950 mS/mm to 1280 mS/mm. The output conductance g_{DS} was reduced especially at low V_{DS}, and the device developed a more distinct knee in the I_{ds} versus V_{DS} with no observed kink behaviour. This should also improve the RF performance of InAs/AlSb HEMTs and make them potential device candidates for cryogenic low-noise amplifiers.

Acknowledgement

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